

Attorney Docket No. 10559-395001
Application No. 09/823,095
Amendment dated March 23, 2004
Reply to office action dated December 23, 2003

Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Previously presented) A method comprising:
storing an instruction and a multiple bit exception status information word, the state of bits of said multiple bit exception word representing multiple different kinds of exceptions; and
issuing the instruction and at least part of the exception status information in parallel.
2. (Previously presented) The method of Claim 1, further comprising:
detecting a width of the instruction prior to said issuing the instruction and at least part of the exception status information in parallel.
3. (Previously presented) The method of Claim 1, wherein said issuing the instruction and at least part of exception status information in parallel comprises:
sending the instruction to a decoder; and

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sending the exception status information through an OR gate to exception handling logic.

4. (Original) The method of Claim 1, further comprising:
fetching at least one data block;
generating exception status information about the data block;
storing the exception status information with the data block; and
detecting at least part of an instruction within the data block.

5. (Original) The method of Claim 4, wherein generating exception status information includes generating information identifying that a particular exception condition was detected.

6. (Original) The method of Claim 4, wherein generating exception status information comprises generating information indicating that a particular exception condition was not detected.

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7. (Original) The method of Claim 4, further comprising:
if only part of the instruction is in the data block,
fetching another data block containing the rest of the
instruction prior to issuing the instruction.

8. (Currently Amended) The method of Claim 7, wherein
said storing the exception status information represents storing
the whole instruction in the multiple data blocks.

9-16. (Canceled)

17. (Currently Amended) A system comprising:
a static random access memory device; and
a processor coupled to the memory device, wherein the
processor includes an execution unit and a control unit, the
control unit including a prefetch unit and exception handling
logic, the control unit ~~adapted~~ operates to:
fetch at least one data block;
generate exception status information about the data block,
the exception status information being a multiple bit exception
status information word, the state of said multiple bit
exception word representing multiple different kinds of
exceptions;

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store the exception status information and the data block
in the prefetch unit;

detect at least part of an instruction within the data
block;

in parallel, issue the instruction to the execution unit
and issue at least part of the exception status information to
the exception handling logic.

18. (Original) The system of Claim 17, wherein the control
unit is further adapted to:

fetch another data block;

generate additional exception status information about the
another data block; and

store the additional exception status information and the
another data block in the prefetch unit.

19. (Original) The system of Claim 17, wherein the
prefetch unit includes at least two prefetch buffers.

20. (Original) The system of Claim 17, wherein issuing the
instruction and at least part of exception status information in
parallel comprises:

sending the instruction to the decoder; and

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sending the exception status information through an OR gate
to the exception handling logic.